### **OpenGPT-X: Training Large Language Models on HPC Systems** JÜLICH

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# **OpenGPT-X (2022 - 2024)**

- German initiative to **build and train** large-scale Al language models for innovative language applications
- **Commercialization** through Gaia-X infrastructure for European Economy
- Consortium of 11 partners from industry and academia





# Large Language Models (LLM)



### LLM Transformer Architecture: Uses stack of encoders/decoders to process data, weighted by attention.

### Use Cases:

- Customer service chatbots
- Translation, autocorrect, autocompletion
- Document summarization and generation
- Insurance claims management
- Fraud detection
- BERT (2018); by Google • GPT models, GPT-1 (2018), GPT-2 (2019), GPT-3 (2020), GPT-4 (2023); by OpenAI
- **OPT** (*2022*), by Meta

Language Models:

- **BLOOM** (2022); by BigScience (*HuggingFace*); based on Megatron-Deepspeed
- **OGPT-1(?)**, by OpenGPT-X, TBD

## **Training 13.6B Model on JUWELS Booster**

### **Model Training**

#### Key Technique: **Parallelization** (memory constraints, large input data)

#### . Distributed Data Parallelism (DP):

- Full model on each rank
- Training data distributed in microbatches
- Gradients averaged across all ranks via allreduce

Global BatchSize =  $\#DP \times Micro BatchSize$ 

#### 2. <u>Pipeline Parallelism (PP)</u>:

- Model layers partitioned across ranks (*vertically*)
- Asynchronous pipe scheduling for gradient accumulation and calculation

### 3. <u>Tensor Parallelism (TP):</u>

- Tensor operations partitioned across ranks (*horizontally*)
- Communication-intensive with frequent *allreduce*
- $\rightarrow$  Use all 3 levels to determine number of tasks / number of GPUs

 $#GPUs = #DP \times #PP \times #TP = #DP \times #MP$ 

#MP

#### **Distributed Data Parallelism**



Example for Distributed Data Parallelism: entire model fits on single GPU. Model processes data in units of micro batches, performs model update with averaged gradients.



Example of different parallelization schemes. MP (Model Parallel) was reformulated to TP, with MP=PPxTP. Parallelization using DeepSpeed ZeRO, https://www.deepspeed.ai/tutorials

- Basis: Megatron-DeepSpeed (fork)<sup>[1]</sup>
- 13.6B Model: 13.6 Billion parameters
- Size: 56 GB (Parameters + Gradients + Optimizer states, *ZeRO Stage* 1<sup>[2]</sup>)
- Partition: #PP=2, to fit 40 GB A100 GPU ( $\rightarrow$ 28 GB per GPU)
- Scaling: #DP=80
- Training on German-English data with GlobalBatchSize=960, MicroBatchSize=2 and GradientAccumulationStep=6
- 160 GPUs (40 nodes) on **JUWELS Booster**<sup>[3]</sup>



Report generated using LLview<sup>[4]</sup>. Training of 13.6B model (TP=1, PP=2 and DP=80): GPU utilisation of 96.3% (avg) making use of 36.6 GB (avg) memory.

#### [1]: Private repository forked from <a href="https://">https://</a> github.com/bigscience-workshop/Megatron-[2]: ZeRO: Memory Optimizations Toward Training Trillion Parameter Models; arXiv:1910.02054 [cs.LG] [3]: JUWELS Booster: > 3200 Nvidia A100 GPUs, 40 GB; https://apps.fz-juelich.de/jsc/hps/juwels/ booster-overview.html [4]: https://www.fz-juelich.de/en/ias/jsc/services/ user-support/jsc-software-tools/llview



Tensorboard: Tokens vs. Training Loss Plot; for 13.6B model trained on 12 billion tokens, 160 GPUs, 24 h. Decreasing loss attests for model quality and convergence.

## **Novel Architecture Exploration**



#### **AMD MI250 GPUs**<sup>[5][7]</sup>



Heatmaps: GlobalBatchSize vs. #Devices Throughput (images per sec) scales with global batch size and Data Parallelism for ResNet-50 model on single node; entire model fits on single device

 $\Rightarrow$  #Devices = #Data Parallelism Graphcore best for small batch sizes, NVIDIA for large; AMD significantly slower (reasons under evaluation)

#### ResNet50 TensorFlow Benchmarking on NVIDIA A100 GPUs, AMD MI250 GPUs and Graphcore GC200 IPUs using ImageNet data on single node



Bar graph comparing (GlobalBatchSize, #Devices) vs. Images per sec (throughput) for ResNet-50 model on NVIDIA<sup>[8]</sup>, AMD<sup>[7]</sup> and Graphcore<sup>[7]</sup> devices on single nodes; entire model fits on single device  $\Rightarrow$  #Devices = #Data Parallelism

- Evaluation of new hardware architectures to test suitability for LLM
- Tests with simple TensorFlow ResNet-50 CNN benchmark using ImageNet data
- NVIDIA/AMD: Stock setup<sup>[5]</sup>
- Graphcore: Vendor/device-optimized setup<sup>[6]</sup>
- Using novel devices of JURECA DC Evaluation Platform<sup>[7]</sup> and JURECA DC<sup>[8]</sup>

[5]: <u>https://github.com/HelmholtzAI-FZJ/tf\_cnn\_benchmarks</u> [6]: https://github.com/graphcore/examples.git [7]: JURECA Evaluation Platform: Additional hardware for benchmarking and testing at JSC [8]: JURECA DC: Pre-Exascale Modular Supercomputer at JSC

#### **Sequence Parallelism:**

• Non-tensor parallel regions of transformer layer are independent along sequence dimension Prevent redundant storage of activations

#### **FlashAttention:**

• Attention algorithm with memory tiling between GPU high bandwidth memory (HBM) and GPU on-chip SRAM

### Challenges

- Scarcity of evaluation tasks in languages other than English
- Availability of quality data

## **Next Steps**

- Ablation studies on training objectives, optimizers and training parameters

- Selective re-computation of activation
- **5× memory reduction** with over 90% compute recovery from full activation re-computation.



Transformer layers with tensor and sequence parallelism. Reducing Activation Recomputation in Large Transformer Models; https://arxiv.org/abs/2205.05198

• 20× memory efficient and faster than standard attention without I/O optimisation

• Block-sparse flash attention is **faster than all implementations** across all sequence lengths



**Left**: Runtime of forward pass + backward pass. **<u>Right</u>**: Attention memory usage. FlashAttention: Fast and Memory-Efficient Exact Attention with IO-Awareness; https://arxiv.org/abs/2205.14135

- Potential model biases
- Limited preprocessing filters for data
- Hardware robustness for large runs
- Energy consumptions: GPT-3 model training used approximately 936 MWh
- GPU communication and offloading using libraries (SHARP, UCC)
- CUDA Graphs
- High Performance Storage Tier NVMe cache<sup>[9]</sup>
- Implement Recent Advancements

[9]: https://apps.fz-juelich.de/jsc/hps/juwels/ cscratch.html#high-performance-storage-tier-cscratch

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